

True Vapor–Liquid–Solid Process Suppresses Unintentional Carrier Doping of Single Crystalline Metal Oxide Nanowires

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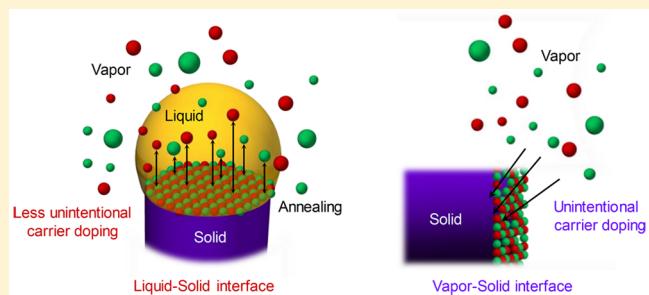
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S Supporting Information

ABSTRACT: Single crystalline nanowires composed of semiconducting metal oxides formed via a vapor–liquid–solid (VLS) process exhibit an electrical conductivity even without an intentional carrier doping, although these stoichiometric metal oxides are ideally insulators. Suppressing this unintentional doping effect has been a challenging issue not only for metal oxide nanowires but also for various nanostructured metal oxides toward their semiconductor applications. Here we demonstrate that a pure VLS crystal growth, which occurs only at liquid–solid (LS) interface, substantially suppresses an unintentional doping of single crystalline SnO₂ nanowires. By strictly tailoring the crystal growth interface of VLS process, we found the gigantic difference of electrical conduction (up to 7 orders of magnitude) between nanowires formed only at LS interface and those formed at both LS and vapor–solid (VS) interfaces. On the basis of investigations with spatially resolved single nanowire electrical measurements, plane-view electron energy-loss spectroscopy, and molecular dynamics simulations, we reveal the gigantic suppression of unintentional carrier doping only for the crystal grown at LS interface due to the higher annealing effect at LS interface compared with that grown at VS interface. These implications will be a foundation to design the semiconducting properties of various nanostructured metal oxides.

KEYWORDS: Metal oxide nanowires, vapor–liquid–solid growth, unintentional carrier doping, crystal growth interface



Single crystalline nanowires composed of semiconducting metal oxides, including SnO₂, ZnO, In₂O₃ and others, have shown their great promises for applications in a variety of fields ranging from energy conversion and electronics to biotechnology due to their unique physical properties and robustness in water and air that are hardly attainable to conventional semiconductors.^{1–6} However, tailoring the electrical conductivity of these metal oxide nanowires has been very difficult due to the occurrence of unintentional doping during crystal growth process.^{7–9} In fact, most nanostructured semiconducting metal oxides in general are electrically conductive even without any intentional doping,^{10,11} although these stoichiometric oxides should be insulators.¹² Suppressing such unintentional doping effect has been a challenging and long-standing issue not only for above single crystalline semiconducting metal oxide nanowires but also for various nanostructured metal oxides toward their semiconductor applications, which require the control of carrier concentration and the bipolarity.^{13–15} Nonstoichiometry properties (e.g., a crystal imperfection) of metal oxides due to the strong ionicity are closely related to the occurrence of such unintentional doping.^{7–11} Note that such

nonstoichiometry exhibits the exotic physical properties of metal oxides, including catalytic, memristive properties, and others.^{16–27} On the contrary, the unintentional doping effect has not been a serious issue for Si, Ge, and III–V nanowires, indicating the inherent difference between ionic metal oxide nanowires and covalent semiconductor nanowires on the occurrence of unintentional doping during crystal growth. Thus, controlling the electrical properties and the unintentional doping effect is an inherent and challenging issue for semiconducting metal oxide nanowires.

Here, we demonstrate that a pure VLS crystal growth in which a solid phase is only formed at LS interface, substantially suppresses an unintentional doping of single crystalline SnO₂ nanowires, which had been impossible by any existing metal oxide nanowire growth methodologies. To achieve the strict growth control, we utilized “material flux window principle”, which describes a relationship between a material flux and a

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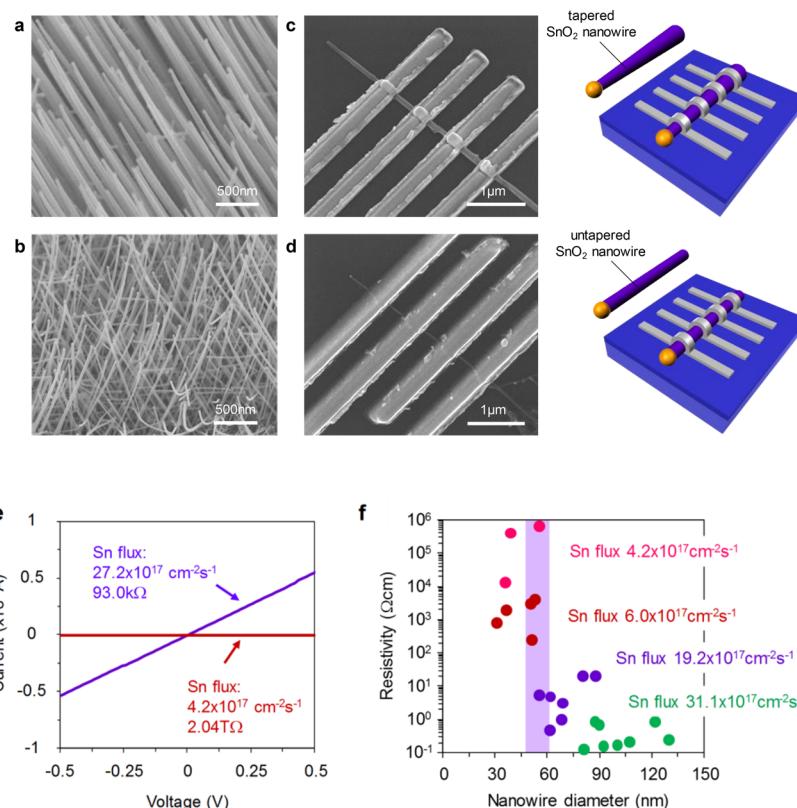


Figure 1. (a) SEM image of tapered SnO₂ nanowires. (b) SEM image of untapered SnO₂ nanowires. (c) Single nanowire electrical measurement device for tapered SnO₂ nanowires. (d) Single nanowire electrical measurement device for untapered SnO₂ nanowires. (e) Comparison between tapered- and untapered nanowires on the electrical measurement (current–voltage data). (f) Statistical data of electrical resistivity when varying Sn flux and nanowire diameter.

nucleation probability of solid at a LS or a VS interface.²⁸ On the basis of this knowledge, we can control the contribution of two crystal growth interfaces (LS and VS) for single crystalline SnO₂ nanowire formation by varying the vapor flux density. Interestingly, the resistance difference between nanowires formed only via LS interface and nanowires formed via both LS and VS interfaces is found to be gigantic up to 7 orders of magnitude (ranged from kΩ to TΩ), although these two nanowires are grown under the same conditions except for the vapor flux density. Spatially resolved single nanowire electrical measurements, plane-view scanning transmission electron microscopy (STEM), electron energy-loss spectroscopy (EELS) analysis, and molecular dynamics (MD) simulations reveal that the unintentional doping via a crystal imperfection can be drastically suppressed at LS interface.

This work is triggered by the discovery of the gigantic difference between tapered and untapered SnO₂ nanowires on the electrical conductivity, as shown in Figure 1. Figure 1a,b shows the scanning electron microscopy (SEM) images of fabricated SnO₂ nanowires when we vary the Sn metal flux (ranged from 10.4 to 27.2 × 10¹⁷ cm⁻² s⁻¹) during nanowire growth. Except for the Sn flux density, these SnO₂ nanowires were grown under the same conditions, including growth temperature (750 °C), oxygen partial pressure (10⁻³Pa), and Au catalyst thickness (~1 nm). The details of nanowire growth can be seen in Methods. Nanowires grown under relatively higher Sn flux (27.2 × 10¹⁷ cm⁻² s⁻¹) showed the tapered nanowire shape, whereas such tapering was not observable for nanowires grown under relatively lower Sn flux (10.4 × 10¹⁷ cm⁻² s⁻¹). Figure 1c,d shows the SEM images of the four-probe

devices to measure the electrical properties of a single nanowire for both tapered and untapered SnO₂ nanowires. Figure 1e shows the comparison between these two nanowires on the electrical properties (current–voltage data). The resistance of untapered SnO₂ nanowire was over 1 TΩ, which is surprisingly 7 orders of magnitude higher than that of tapered nanowire (93.0 kΩ). To further reveal the statistical difference between tapered and untapered SnO₂ nanowires on the electrical conduction, Figure 1f shows the distribution of measured electrical resistivity when varying the Sn flux and the nanowire diameter. As clearly seen in the figure, there is a significant difference between tapered and untapered SnO₂ nanowires on the single nanowire electrical resistivity. The electrical resistivity showed the difference of 5 orders of magnitude in the nanowire diameter range around 50 nm when varying the Sn flux. Considering the fact that these tapered and untapered nanowires were grown under thermodynamically similar conditions except for the Sn flux, this observed difference is gigantic. Thus, varying slightly Sn flux strongly affects not only the tapering of nanowire shape but also the electrical properties of SnO₂ nanowires during VLS growth.

Above tapering phenomena of nanowires grown via VLS process can be interpreted in terms of the competition between a crystal growth at VS interface on the nanowire sidewall (VS growth) and a crystal growth at LS interface (LS growth).²⁹ This is also consistent with so-called “material flux window”, which describes the concept of VLS nanowire growth within a limited material flux range, where a nucleation preferentially occurs only at the LS interface.²⁸ In this principle, increasing the Sn flux should tend to promote the VS growth, resulting in

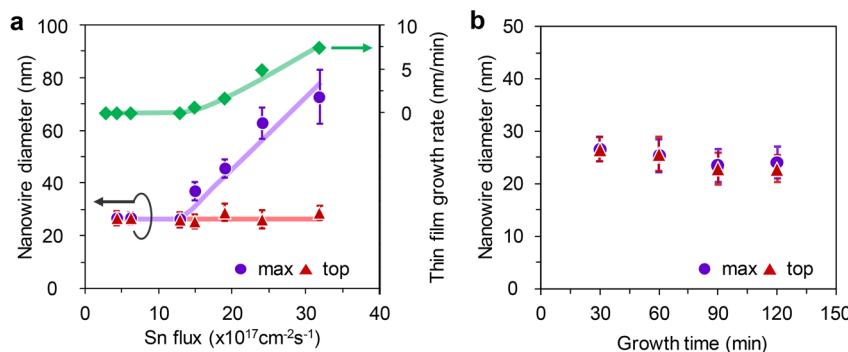


Figure 2. (a) Sn flux dependence on SnO_2 nanowire morphology (diameter) and SnO_2 film growth rate. (b) Growth time dependence of nanowire diameter. These SnO_2 nanowires were grown under same the conditions, including growth temperature (750°C), oxygen partial pressure (10^{-3} Pa), and Au catalysts thickness (~ 1 nm).

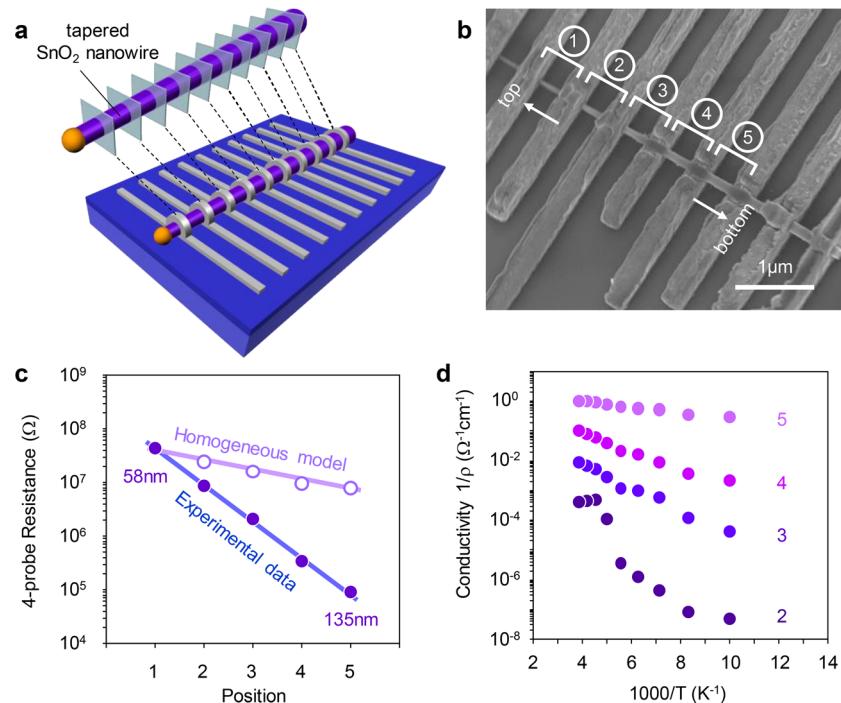


Figure 3. (a) Schematic illustration of multielectrodes devices to measure the spatial electrical distribution of a tapered SnO_2 nanowire. (b) SEM image of multielectrodes devices to measure the spatial electrical distribution of a tapered SnO_2 nanowire. (c) Spatial distribution of 4-probe electrical resistance for a tapered SnO_2 nanowire with calculated values for spatially homogeneous model. (d) Spatial distribution of temperature dependent 4-probe electrical resistance for a tapered SnO_2 nanowire.

the tapering of nanowire shape, which is consistent with above our results. To ensure this tapering effect in our system, we measured the morphology of nanowires when varying the Sn metal flux. Figure 2a shows the Sn flux dependences on both the diameter value near the tip and the maximum diameter value at the bottom. Above $15 \times 10^{17} \text{ cm}^{-2} \text{s}^{-1}$ of the flux, the tapering occurred, where the maximum diameter value tends to increase whereas the diameter near the tip was independent of the flux variation. To more clearly reveal the role of VS growth on these diameter data, we measured the Sn flux dependence on the VS film growth rate in the absence of Au catalysts, as shown in Figure 2a. These films were grown under the same growth conditions of nanowires. Below $15 \times 10^{17} \text{ cm}^{-2} \text{s}^{-1}$ of the flux, there was almost no VS film growth, and the film growth rate increased as the flux increased above $15 \times 10^{17} \text{ cm}^{-2} \text{s}^{-1}$. Clearly, the Sn flux dependence of VS growth can well explain the tapering phenomena of the present SnO_2

nanowires in terms of the competition between VS growth and LS growth. To further reveal the absence of VS growth for untapered SnO_2 nanowires, we measure the growth time dependence of diameters for untapered nanowires because the diameter of untapered nanowires should increase with the growth time if the untapered SnO_2 nanowires are formed at both LS and VS interface. The results are shown in Figure 2b. As can be seen, the diameter for untapered nanowires is almost consistently independent of the growth time. Thus, the crystal growth at VS interface for untapered nanowires is almost negligible, which is also consistent with the results of Figure 2a. All our experimental results consistently support the absence of crystal growth at VS interface for untapered SnO_2 nanowires. These results highlight that we can strictly control the crystal growth interface including VS interface and/or LS interface during the VLS nanowire growth of SnO_2 by varying the Sn metal flux. Thus, overall experimental trends of Figure 1 and

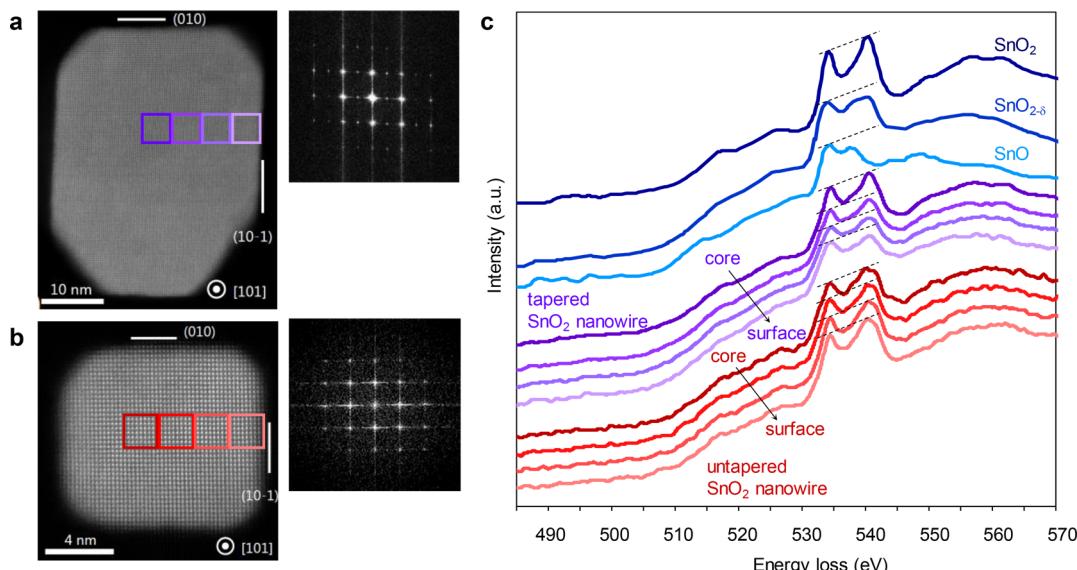


Figure 4. (a) Plane-view STEM image of tapered SnO_2 nanowire. (b) Plane-view STEM image of untapered SnO_2 nanowire. (c) Spatial distribution of EELS spectra for both tapered SnO_2 nanowire and untapered SnO_2 nanowire with reference EELS spectra for SnO , SnO_2 , and $\text{SnO}_{2-\delta}$.

Figure 2 imply that enhancing the VS crystal growth at nanowire sidewall (i.e., the tapering) seems to strongly impact the electrical transport properties of a single SnO_2 nanowire.

Here we consider the following three possible scenarios to explain the gigantic difference between the tapered and untapered SnO_2 nanowires on the electrical transport properties in Figure 1e,f. The first scenario is based on the nanowire diameter difference, which explains the nanowire resistance variation in terms of the cross-sectional area difference by assuming the spatially homogeneous electrical conductivity. Second scenario assumes the spatially inhomogeneous conduction model based on the presence of insulating depletion layer near the nanowire surface, which explains the resistance increase for the smaller nanowires. Third possible scenario assumes the conductive shell layer formed via VS interface and the insulative core crystals formed via LS interface. The illustration of these three models is shown in Supporting Information S1. To examine the first scenario, we measure the electrical resistivity of a single nanowire when varying Sn flux, as shown in Figure 1f. As can be seen in Figure 1f, increasing the Sn flux value consistently decreases the resistivity value. Thus, the observed Sn flux dependence on the electrical transport properties cannot be interpreted solely in terms of the diameter variation via tapering. This excludes the first scenario based on only the nanowire diameter difference with the spatially homogeneous electrical conductivity.

To further validate above three scenarios, we measured the spatial distribution on the electrical transport properties of tapered SnO_2 nanowires by using multielectrodes, as shown in Figure 3a,b. The tapering effect (i.e., VS growth effect) on the electrical properties must be less significant as the measured spatial position approaches to the tip of nanowire. Figure 3c shows the spatial distribution data of 4-probe resistances within the single tapered SnO_2 nanowire. Figure 3d shows the temperature-dependent electrical conductivity. As can be seen, there was the strong spatial dependence of nanowire resistance, which was ranged from 10^4 to $10^7 \Omega$. As the measured spatial position tends to be away from the tip of tapered nanowire, the resistance tended to decrease and the temperature dependence tended to be metallic from semiconducting. Considering the

relatively short spatial distance within $3 \mu\text{m}$ for this single nanowire transport measurement, the observed 3 orders difference of resistance values and the different temperature dependence for different electrode gaps were rather gigantic. In the first and second scenarios, the diameter dependence of nanowire resistance should be approximately proportional to $1/\text{diameter}^2$. This is because these two scenarios assume the conductive inner layer, whose cross-sectional area increases with increasing the nanowire diameter. The third scenario's diameter dependence of nanowire resistance can be stronger, which depends on the resistivity difference between the crystal grown at VS interface (VS crystal) and the crystal grown at LS interface (LS crystal), and also the cross-sectional area ratio of each crystal. To examine this, we measured the spatial diameter variation within a single nanowire in SEM image. Figure 3c also shows the comparison between experimental data and expected diameter dependence of homogeneous model. The experimental diameter dependence on the nanowire resistance did not conform to $1/\text{diameter}^2$ of spatially homogeneous model, and the diameter dependence is much stronger than $1/\text{diameter}^2$. In addition, all spatially resolved single nanowire measurements showed that the nanowire resistivity tended to be lower as the measured spatial position tended to be away from the tip, where VS crystal tended to be dominant. This implies the significant role of outer VS crystal on the electrical transport properties. Note that the similar gigantic resistance variation within a single tapered SnO_2 nanowire was also observed even when we varied the oxygen partial pressures to promote the VS growth instead of the variation of Sn flux, as seen in Supporting Information S2. Thus, these spatially resolved resistance measurement data within the single tapered SnO_2 nanowire consistently support the third scenario, which assumes the conductive outer VS crystal and the rather insulative inner LS crystal, to explain the gigantic difference of nanowire resistance when varying the Sn metal flux in Figure 1e.

Next, we question what is essentially different between LS crystal and VS crystal. Because X-ray diffraction and ultraviolet-visible (UV-vis) light absorption spectra data can not reveal the spatial difference between the two crystals (see

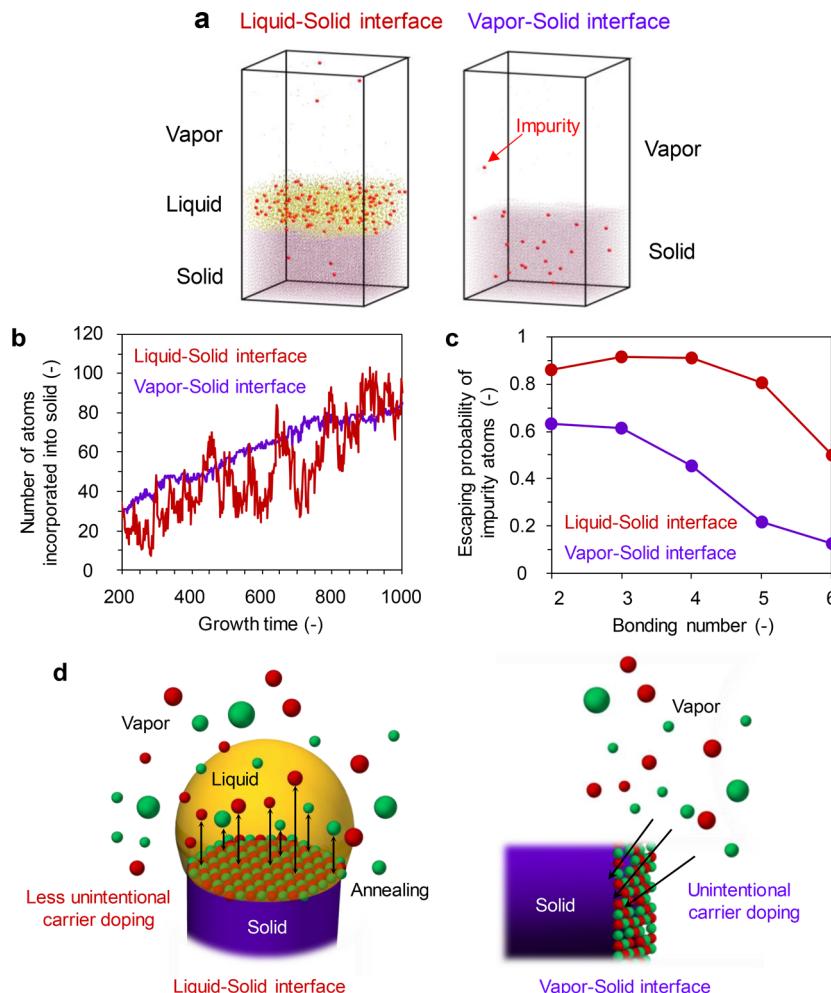


Figure 5. (a) Snap shots of crystal growth MD simulations for both LS interface and VS interface in the presence of impurity atoms. (b) Time evolution data of crystallized atom numbers for both LS interface and VS interface. (c) Escaping probability data of impurity atoms from a solid phase into a liquid or vapor phase during crystal growth as a function of bonding number. (d) Schematic illustration of an inherent difference between LS interface and VS interface on an unintentional carrier doping during crystal growth.

Supporting Information S3 and S4), we performed plane-view STEM-EELS analysis. The details of STEM-EELS measurements can be seen in Methods. Figure 4a,b shows the plane-view annular dark field (ADF) STEM images of tapered and untapered SnO_2 nanowires. Both plane-view STEM images consistently showed the single crystallinity, and the different cross-sectional nanowire shapes are due to the occurrence of VS growth on the sidewall of nanowires. To observe the difference between LS crystal and VS crystal, we have performed spatially resolved EELS analysis, and the spatial spectra data of both tapered and untapered SnO_2 nanowires are shown in Figure 4c. For comparison, the reference spectra³⁰ of SnO_2 , $\text{SnO}_{2-\delta}$, and SnO are shown. For untapered nanowire, there was no spatial dependence of the O–K edge spectra data, which well agrees with the reference spectra data of stoichiometric SnO_2 . On the other hand, for tapered nanowire the O–K edge EELS spectra data exhibited the spatial dependence. The spectra data near the outer layer tends to be closer to the reference data of oxygen-deficient $\text{SnO}_{2-\delta}$, whereas the spectra data of inner core is very consistent with the reference data of stoichiometric SnO_2 (see more details in Supporting Information S5). This crystal imperfection, including oxygen deficiencies and related other dopant incorporations, seems to play an important role on the

unintentional doping of SnO_2 during crystal growth, although the exact origin of unintentional doping in SnO_2 has been a long-standing issue and controversial.^{31,32} As to the relationship between such crystal imperfections–oxygen vacancies and the electrical conductivity for SnO_{2-x} we measure the electrical resistivity of SnO_{2-x} films when varying the oxygen partial pressure during film formation; see the details in Supporting Information S7. Results imply that there is a certain correlation between crystal imperfections–oxygen vacancies and the electrical conductivity of SnO_{2-x} . These STEM-EELS results highlight that the tapered SnO_2 nanowire is composed of the outer VS crystal layer, which contains crystal imperfections, including oxygen deficiencies, and the inner more stoichiometric LS crystal core.

Finally, we question why there is a significant difference between LS crystal and VS crystal on the electrical conductivity via the crystal imperfection and/or the impurity incorporation dynamics during a VLS nanowire growth of SnO_2 . Because it is rather difficult to experimentally observe the impurity incorporation dynamics, we qualitatively examine this issue by performing molecular dynamics (MD) simulation. The details of MD simulations can be seen in Methods and Supporting Information S6. In these MD simulations, we intentionally employ impurity atoms to examine the impurity incorporation

dynamics into LS crystal or VS crystal. In the following simulations, the relative interaction parameter of impurity ϵ' is set to be $\epsilon' = 0.8 (<1)$, where the incorporation of impurity atoms into the solid phase destabilizes the solid structure. **Figure 5a** shows the snapshots of performed MD simulations for both LS crystal and VS crystal. As illustrated in **Figure 5a**, the impurity incorporation into the solid phase tends to be more difficult for LS interface growth when compared with VS interface growth. To understand this difference on the impurity incorporation dynamics in terms of the growth dynamics, we calculated the time tracking data of the number of atoms participating the crystal growth in MD simulations, as shown in **Figure 5b**. The time tracking data of both LS crystal and VS crystal were shown for the comparison. As the crystal growth continues, the number of crystallized atoms increases for both crystals. One of the clear difference between LS crystal and VS crystal on the time tracking data is a fluctuation in the number of crystallized atoms. The number of crystallized atoms at LS interface is more fluctuated than that at VS interface, highlighting that the growing layer at the solid surface is more frequently reconstructed at LS interface. **Figure 5c** shows the difference between LS interface and VS interface on the escaping probability of impurity atoms from the solid phase into vapor or liquid phase during crystal growth. At LS interface, an impurity atom once incorporated into the solid phase can be more effectively ejected into liquid phase, compared with the ejection of impurity atoms to vapor phase at VS interface. In consequence, excessive impurity atoms are well released from the solid phase, and more pure solid structure can be grown at LS interface, which is in contrast to the VS interface where unintentional crystal imperfections remain. This effect is very similar to an annealing effect when we anneal the samples to improve the crystallinity and purity.^{33–35} In general, atoms are more frequently exchanged between liquid and solid phases, when compared to that between vapor and solid phases. This is because the effective energy per atom is lower in the liquid than in the vapor phase when the liquid has high affinity with the atoms. This kind of annealing effect enhanced by liquid phase and the improvement of the crystallinity should generally occur at LS interface. Thus, these MD simulations qualitatively demonstrate that an unintentional doping of VLS nanowires can be suppressed by intentionally forming the crystal only at LS interface without the crystal at VS interface, as illustrated in **Figure 5d**.

The present results highlight that we can tailor the previously unavoidable unintentional carrier doping of nanostructured semiconducting metal oxides by utilizing the pure VLS crystal growth only at LS interface. The resistivity values of present well-defined SnO₂ nanowires are almost 3–4 orders of magnitude higher than those of previously reported single crystalline SnO₂ nanowires (see *Supporting Information S8*). For this well-defined VLS process, the metal catalysts play a role of filtering to exclude impurity atoms from fabrication environments. In other words, it is possible to fabricate high-purity semiconducting metal oxide nanostructures even under relatively “dirty” and cheap fabrication circumstances compared to conventional semiconductor fabrication technologies, which require ultraclean and expensive growth processes. MD simulations predict that this strategy should be applicable for various semiconducting metal oxide nanostructures if the crystal growth is designed to occur only at LS interface via VLS process. The present knowledge can be extended to further tailor the semiconducting properties and heterostruc-

tures (e.g., bipolarity and pn junctions) of various functional semiconducting metal oxide nanostructures.

We have shown that a pure VLS crystal growth only at LS interface substantially suppresses an unintentional doping of single crystalline SnO₂ nanowires. By strictly tailoring the crystal growth interface of VLS process, we found the gigantic electrical conduction difference (up to 7 orders of magnitude) between nanowires formed only at LS interface and those formed at both LS and VS interfaces. Spatially resolved single nanowire electrical measurements revealed the occurrence of preferential unintentional doping only for the crystal growth at VS interface. Plane-view STEM-EELS analysis clarified the crystal imperfection of outer-layer of nanowires, formed at VS interface, which was not observable for nanowires formed at LS interface. MD simulations qualitatively explain why such unintentional doping preferentially occurs only at VS interface and not at LS interface in terms of the annealing effect enhanced at LS interface. These implications will be a foundation to further tailor the semiconducting properties not only of single crystalline metal oxide nanowires but also of various functional metal oxide nanostructures.

Methods. Fabrication of SnO₂ Nanowires. SnO₂ nanowires were grown onto a sapphire Al₂O₃(110) substrate (Electronics and Materials) by pulsed laser deposition method, as reported elsewhere.^{36–38} Prior to nanowire growth, Au layer (~1 nm) was deposited onto the substrate by utilizing direct current sputtering (SANYU Electron, SC-701HMC). A laser ablation with ArF excimer laser ($\lambda = 193$ nm, Coherent, COMPex Pro) was performed to supply the vapor source. SnO₂ tablet (99.99% pure, Kojundo Chemical Laboratory) was used as the target. For the nanowire growth, the chamber was first evacuated to be less than 5×10^{-5} Pa, then the oxygen/argon mixture gas (99.9999% pure) was introduced by controlling the oxygen partial pressure in the range of 10^{-4} –10 Pa. The total pressure of 10 Pa was kept in order to prevent the catalyst consumption during the nanowire growth.³⁹ Before the laser ablation, the substrate temperature was heated up to 750 °C within 20 min and kept constant during the nanowire growth. The repetition rate, the laser energy, and the target-to-substrate distance were 10 Hz, 40 mJ, and 30 mm, respectively. The flux of vapor species was controlled by varying the energy density (mJ/mm²) of laser ablation. The duration of nanowire growths was 30–300 min. After the nanowire growth, the substrate temperature was cooled down to room temperature within 30 min. The Sn flux was quantitatively evaluated via film deposition at room temperature in 10 Pa O₂ atmosphere. After measuring the thickness of the obtained thin film using a surface profiler (KLA Tencor, Alpha-Step IQ), the material flux was estimated using the density of the element.

Nanowire Characterizations. The morphology of obtained SnO₂ nanowires was evaluated by a field-emission scanning electron microscopy (FESEM, JEOL, JSM-7610F) at accelerating voltage of 15–30 kV. The diameter and the length of nanowires were statistically evaluated from 100 nanowires. We employed a scanning transmission electron microscopy (STEM, JEOL, JEM-ARM300F) equipped with electron energy loss spectroscopy (EELS, GIF Quantum), at accelerating voltage of 300 kV. A Cu microgrid covered with lacey C film was used to support the nanowire samples for the STEM measurements. The probe size was approximately 0.06 nm. Acquisition time of EELS spectra was 45 s for each pixel. During the acquisitions, the probe scanned inside pixel. In order to correct energy drift due to instability of the

microscope, the zero-loss peak was simultaneously obtained at each core-loss acquisition. Because the original reference spectra in Figure 4 are not calibrated, they were offset to align the oxygen first peak. The smoothed spectra were obtained by weighted average method with 1 eV window. X-ray diffraction (XRD, Philips, X'Pert) was employed to evaluate the averaged crystallinity of nanowires on the substrate. Ultra-violet–visible (UV–vis) absorption spectroscopy (Shimadzu, UV-2400) was performed in the wavelength range of 190–900 nm. The absorption spectra of the SnO₂ nanowires were obtained by subtracting the background signals from the sapphire substrate.

Electrical Transport Measurements. The electrical transport measurement of SnO₂ nanowires was conducted with a form of single nanowire device, which was constructed onto SiO₂/Si substrate by 30 kV electron beam (EB) lithography technique.^{40,41} For the SiO₂/Si substrate, thermally oxidized 100 nm thick SiO₂ was capped on the degenerated p-type Si (100) substrate (resistivity $\sim 1\text{--}5 \times 10^{-3}$ Ωcm). EB lithography process was performed by utilizing ZEPS20A-7 (ZEON) as a resist. First, the nanowires grown onto sapphire substrate were dispersed into isopropanol by sonication with frequency of 28 kHz for 1 min. Then 1 μL of the nanowire suspension was dropped onto the SiO₂/Si substrate with prepatterned microelectrode. EB lithography was performed to bridge between the nanowires and the microelectrodes. For the electrical contact, Pt was deposited via a custom-ordered RF magnetron sputtering (SEINAN) at 50 W in Ar 0.3 Pa. The Pt thickness was controlled to be about 150 nm. Finally, the resist capped with Pt film was lifted-off by *N,N*-dimethylformamide followed by the cleaning in acetone. The electrical transport measurements were performed in the probe station (Lake Shore Cryotronics, Model TTPX) connected with a semiconductor parameter analyzer (Keithley, 4200SCS) at temperature range of 100–300 K in vacuum condition ($<10^{-2}$ Pa).

Molecular Dynamics (MD) Simulations. The molecular dynamics (MD) simulation can express time-evolution of motion (position and translation speed) for each of particles which interact with each other through short-range Lennard-Jones (L-J) interaction.^{42–44} In this simulation system, four types of particles (A, B, A', and C) were utilized to model vapor–liquid–solid (VLS) growth process. Here, A and C can make AC compound in solid phase that expresses an oxide formation, A' is an impurity atom, and B is assigned as solvent liquid atom. L-J type potential is used as two-body interaction potential except that the interaction between A–A and C–C. More details of calculations and employed formulas can be seen in Supporting Information S7.

■ ASSOCIATED CONTENT

● Supporting Information

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Additional information and figures ([PDF](#))

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Notes

The authors declare no competing financial interest.

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