Supporting information for

Modulation of Thermoelectric Power Factor via Radial Dopant Inhomogeneity in B-doped Si Nanowires

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Contents:

1. Device configuration for Seebeck coefficient measurement

Figure S1 (a) shows the device configuration to measure the resistivity (ρ) and Seebeck coefficient (S) for B-doped silicon nanowires. The micro-heater, 2 resistive thermometers and several additional electrodes for 4-probe method were fabricated. The device was fabricated on Si substrates with 300nm SiO_2 layer. The electrodes were composed of Pt, which provided an ohmic contact with the present B-doped Si nanowires.

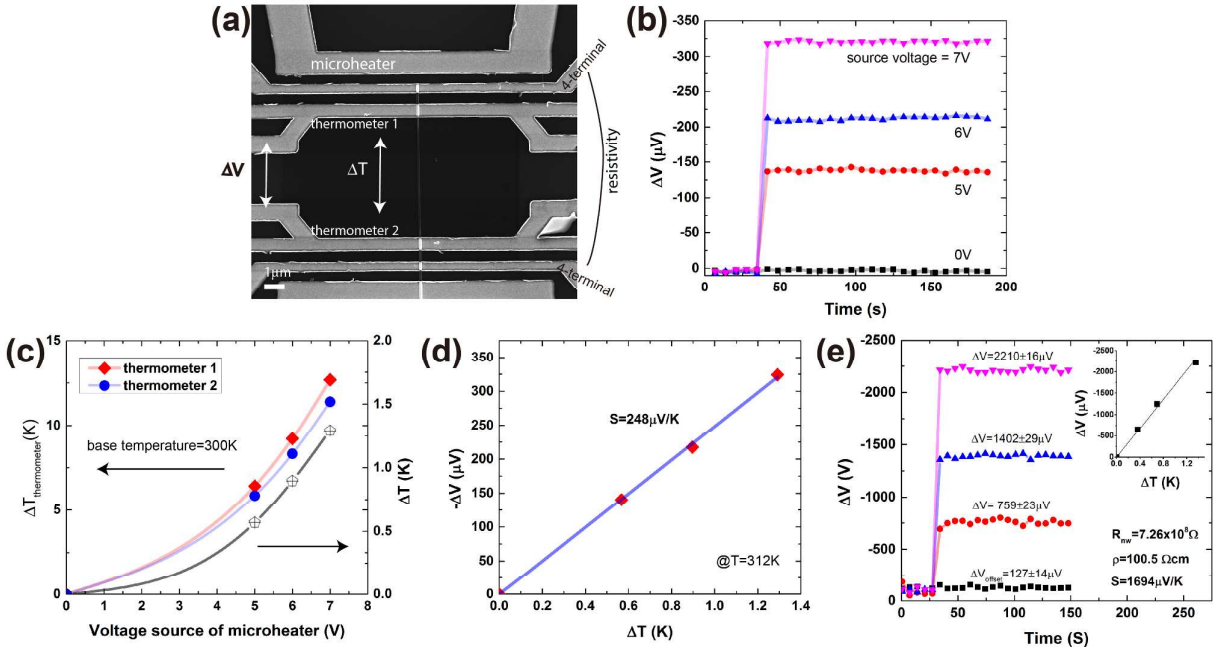

Figure S1. a) The nanowire device configuration for resistivity and Seebeck coefficient measurements. b), c) and d) show the typical data of thermovoltage (ΔV) measurement, temperature (ΔT) calibration and linear regression between ΔV~ΔT for thermopower S. The source voltages of microheater for these measurements were varied from 5 to 7V to induce different temperature gradient. e) shows the example of Seebeck measurements on highly resistive nanowires.

Seebeck coefficient values were determined by using the microheater and the thermometer electrodes. During measurements, the microheater was heated up to induce a temperature gradient by applying a constant voltage. The thermovoltage (ΔV) along the Si nanowire was then recorded by using the thermometer electrodes (with the thermometer-2 grounded). Subsequently, the temperature difference (ΔT) was measured by tracking the resistivity variation of the two Pt thermometers. Figure S1 (b) and (c) show the extracted thermovoltage and temperature data under various source voltages on the micro-heater. A linear fit of the measured ΔV and ΔT was then used to determine the Seebeck coefficient value of the Si nanowire, S=-$\Delta V/\Delta T$, as shown in figure S1 (d). We note that the final S reported in this study was further corrected by subtracting the thermopower of Pt electrodes (S_{Pt}~-

5μV/K),[1] although its contribution was almost negligible in the present experimental range. To perform above measurements, a cryostat system equipped with microprobes and Keithley 4200SCS (with preamplifier KI4200) was used. The high input impedance of the voltage measurement system (>10^{18}Ω) allowed reliable Seebeck measurement even on those highly resistive nanowires, as shown in figure S1 (e). The estimated offset voltage and noise level in the measured voltage signal was generally 10~150μV and <30μV. Before the measurements, the cryostat was evacuated to a pressure below 0.1Pa.

To extract the temperature difference ΔT on Si nanowires, the temperature coefficient of resistivity (TCR) of Pt thermometer of ~0.35% was used. This value was obtained by averaging data on different devices. The raw resistance data from different thermometers was shown in figure S2. The measured TCR value was found slightly lower than the standard value (~0.385%) of high purity Pt on Al_2O_3 substrates.[2]

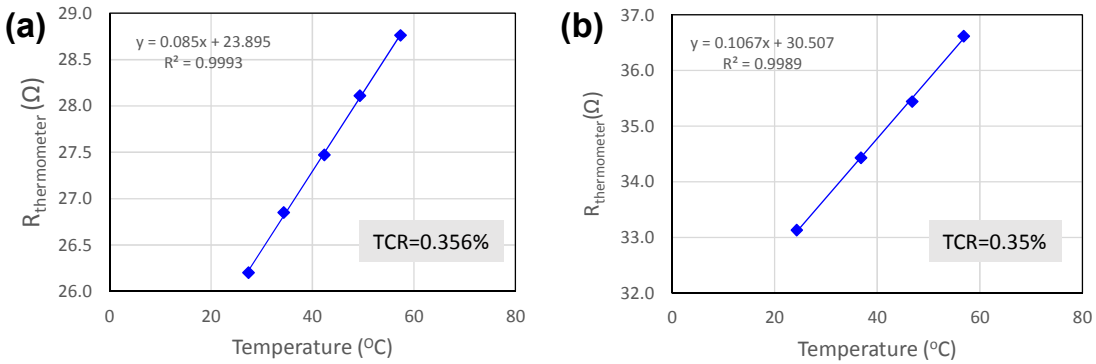

Figure S2. a), b) The TCR calibration of Pt thermometers using the measured temperature dependent resistance in the range of 300~330K. The measured TCR was ~0.35% by referencing to the extrapolated resistance at 0°C.

2. Diameter calibration of Si nanowires by SEM and TEM

In this study, we measure the diameter of Si nanowires by SEM (JEOL JSM 7001F). To evaluate the accuracy of this estimation, we compare the SEM data with the size measured from TEM observation for the same nanowires. To be able to do this, the nanowire device was made on a suspended Si_3N_4 membrane. The fabrication process and corresponding results were shown in Figure S3. The Si_3N_4 was 50nm thin, which was sufficient for the transmission of electron beam. By comparing the SEM and TEM observation, we have obtained the correlation between the two, as shown in Figure S3 (f). As can be seen, the diameter sizes measured by SEM were over-estimated by ~2.8nm in the average, when compared with TEM data.

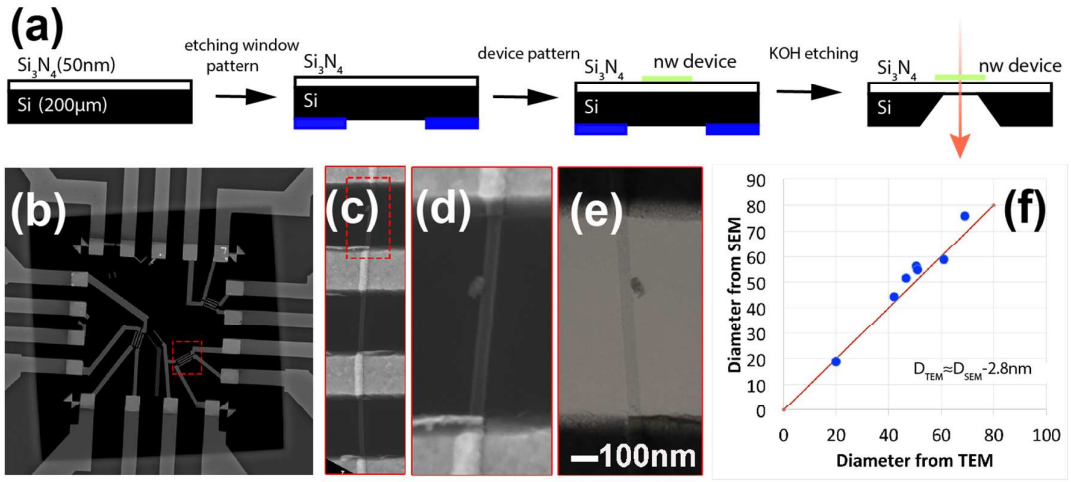

Figure S3. (a) Fabrication procedure of Si nanowire devices on Si_3N_4 membrane substrate for TEM observation. (b), (c) and (d) show the SEM images of fabricated Si nanowire devices on Si_3N_4 membrane. Image (e) shows the corresponding TEM image taken at the same position with (d). Figure (f) shows the comparison between SEM and TEM measurements on the estimated diameters of Si nanowires.

3. System error estimation

3.1 Resistivity

The electrical resistivity ρ was determined from the measured nanowire resistance R and diameter d via $\rho=R\pi d^2/4L$, where L is nanowire length between electrodes. Since the resistance contribution from the contact (Si/Pt) was generally eliminated by the 4-probe method, the major error in the resistivity determination came from the measurement accuracy of diameter. From the calibration shown in Figure S3, we expected a ~5% overestimation in the diameter (+2.8nm for a 50nm).

3.2 Seebeck coefficient

Both the thermovoltage and temperature measurements determine the overall error of estimation for the Seebeck coefficient values. The standard error for voltage measurements depended on the impedance match between the nanowire and measurement system. With the high impedance Keithley 4200SCS, this error was found to be less than ~5% in our system. The temperature measurements depended on the accuracy of the resistance measurement of thermometer. In our experiments, the standard error for the 4-probe resistance measurement on Pt thermometer was found around 0.002~0.01Ω. Considering the total resistance of the thermometer (30~50Ω), an uncertainty of <0.03K was estimated for the temperature measurement. Such accuracy was comparable with the commercial thermocouples based on resistivity calibration. Considering these factors and the

variation of TCR of Pt thermometers (0.35±0.025%) among different devices, we estimated an overall error of ~10% in the measured Seebeck coefficient data. This percentage error has been reflected in the figures in manuscript.

4. Resistivity distribution of VLS grown B-doped Si nanowires

We were able to obtain the statistical information of electrical resistivity of present VLS grown Si nanowires by measuring over 60 nanowire devices. Figure S4 shows the nanowire resistivity data versus the diameter. The frequency distribution of resistivity data was shown in the inset. As seen in the figure, the present Si nanowire exhibited the wide distribution in the electrical resistivity, ranging from $3\times10^{-3}\Omega$cm to $6\times10^{2}\Omega$cm. Especially, there was no significant size dependence on the nanowire resistivity data. In this case, the impurity scattering from ionized dopant atoms still dominates over the surface scattering, and the size effect (including the quantum effect) on resistivity seems to be negligible within the present experimental conditions.[3]

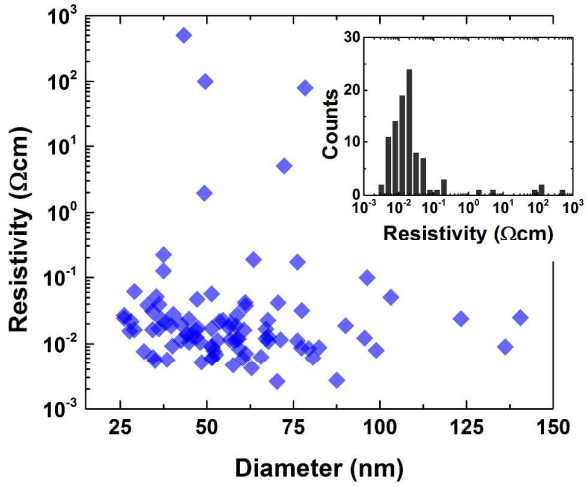

Figure S4. Nanowire resistivity data as a function of the diameter for the present B-doped Si nanowires. The inset shows the frequency of resistivity data ranging from 10^{-3} to $10^{3}\Omega$cm.

5. Seebeck coefficient of homogeneously doped Si

The Seebeck coefficient S of semiconductor is generally consisted of both the electronic and phonon drag part, $S=S_d+S_{ph}$. The electronic part S_d can be obtained by solving the Boltzmann transport equation based on the known electronic band structure of Si. The second phonon drag term S_{ph} comes from the phonon-electron interaction, and is usually described as $S_{ph}=\beta v_{ph} l_{ph}/\mu_e T$.[4, 5] In this formula, v_{ph} and l_{ph} are respectively the velocity and mean free path (MFP) of phonons, μ_e is the electron mobility, and β is the interaction coefficient.[4] The mean free path of phonons can be

modulated by the presence of surface/interface or impurities scatterings. In Si nanostructures, l_{ph} is usually greatly reduced due to the strong space confinement. Thus, S_{ph} contribution to the total S tends to be minor. Considering the average diameter of present nanowires (~50nm) and l_{ph} in bulk Si (~1μm),[5] we expected S_{ph} was decreased by 20 times in our nanowires. This would lead to a negligible S_{ph} of ~20μV/K even in the most resistive Si nanowires. With the minor contribution of S_{ph}, the total S in Si nanowires can be then approximated by the electronic part S_d. By solving the Boltzmann transport equation, S_d has been well modeled and can be expressed by the Mott relation. For non-degenerate semiconductors, it was further simplified as

$$S_d = \frac{k_B}{e}\left(\frac{E_F - E_V}{k_B T} + \lambda + \frac{5}{2}\right)$$

where k_B is the Boltzmann constant, E_F and E_V are respectively the energy of Fermi level and valence band edge, λ is the scattering factor and is -1/2 when the phonon scattering dominates impurity scattering during hole transport.[4] In this work, the above non-degenerate assumption was used for the Si nanowires with carrier concentration of less than $1\text{x}10^{18}\text{cm}^{-3}$.

From the above equation, the Seebeck coefficient of Si can be described by the Fermi level, which can be further derived from the carrier concentration p by using the well-known relation: $p=N_V*exp(-(E_F-E_V)/k_BT)$, where N_V is the effective density of states in valence band. Hence, the theoretical relation of S_d~p can be simply obtained by conducting the above calculation under various doping levels. To obtain the desired S_d~ρ relation as the measured results, the carrier concentration p was further replaced by the electrical resistivity $\rho=p\mu e$ by using the empirical hole mobility of B-doped Si,[6]

$$\mu = \mu_0 e^{-\frac{p_c}{p}} + \frac{\mu_{max} - \mu_0}{1 + (p/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/p)^{\beta}}$$

All the parameters used in this calculation were listed in table S1, which were obtained from the numerical fitting of the experimental measured hole mobility in bulk Si.[6] A good consistency can be found between the calculated S_e~ρ relation and the earlier reported data on homogeneously B-doped Si (Figure 2 of the main manuscript).

Table S1. A list of the parameters used for the calculation of S_e~ρ relation.

Parameter	N_v	μ_0	μ_{max}	μ_1	C_r	C_s	α	β	p_c
Value	$1.04\text{x}10^{19}$	44.9	470.5	29.0	$2.23\text{x}10^{17}$	$6.10\text{x}10^{20}$	0.719	2.00	$9.23\text{x}10^{16}$
Unit	cm^{-3}	cm^2/Vs	cm^2/Vs	cm^2/Vs	cm^{-3}	cm^{-3}	/	/	cm^{-3}

6. FET mobility evaluation under back-gate configuration

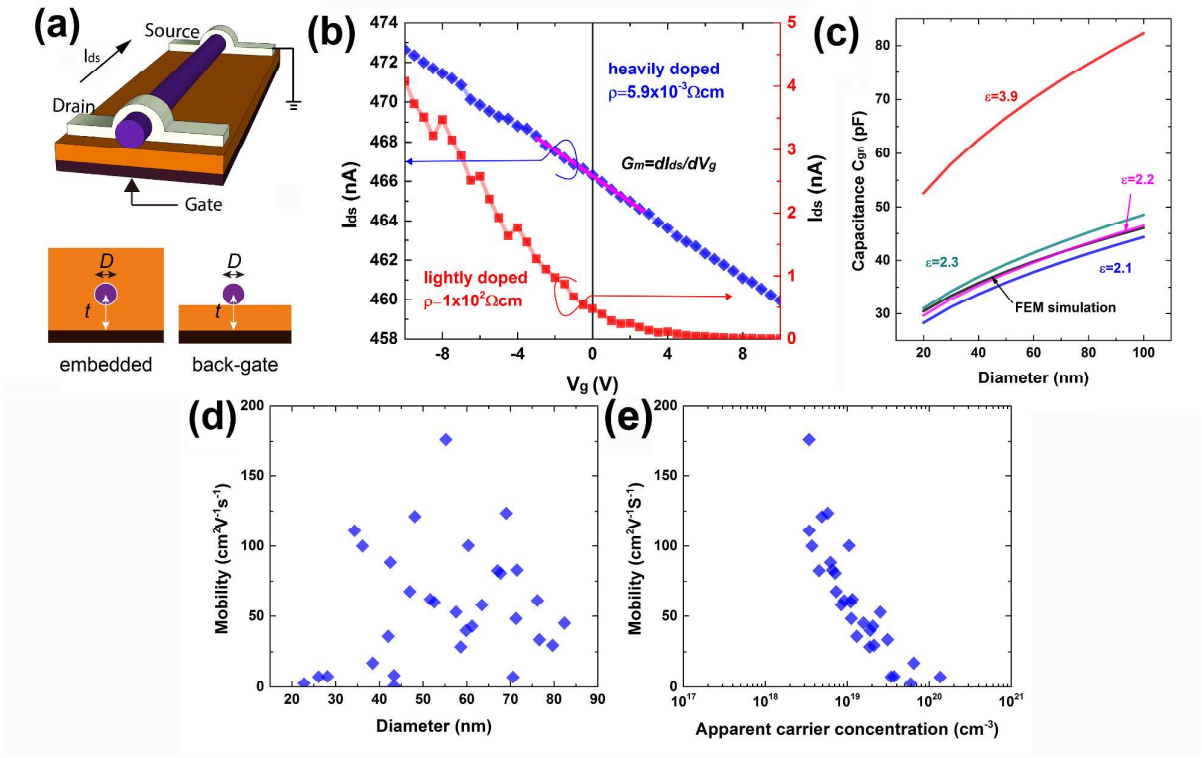

Figure S5. (a) Illustration of the back-gate configuration for the determination of hole mobility in Si nanowires. (b) Typical examples of field effect measurements on B-doped Si nanowires under a small source-drain bias of V_{ds}=0.02V. (c) A comparison between the device capacitance estimation from the analytical method (with various dielectric constant assumed) and FEM simulation. (d) and (e) shows the extracted hole mobility plotted versus the nanowire diameter and the derived carrier concentration.

The hole mobility of Si nanowire was estimated by performing FET measurements using the back-gate configuration (shown in Figure S5 (a)). The typical gate modulated drain current I_{ds} for a heavily and a lightly B-doped Si nanowires are shown in Figure S5 (b). The hole mobility in Si nanowire was determined from the slope of dI_{ds}/dV_g around the zero bias, as $\mu_h=(dI_{ds}/dV_g)*L^2/(C_{gn}V_{ds})$, where L is the nanowire length, C_{gn} is the gate-nanowire capacitance.[7, 8] As shown in the figure, the observed gate dependences of present Si nanowires were consistent with the behaviors of *p*-type semiconductors. Under negative biased gate voltage, holes were induced within the nanowire, which increased the source-drain current. However, with the small physical dimension of nanowires, the direct measurement of C_{gn} is usually very challenging. Here, we used the analytical approximation based on the metallic cylinder-on-plate model.[9] The capacitance of an embedded metallic nanowire can be written as $C_{gn}=2\pi\varepsilon_0\varepsilon_r L/cosh^{-1}(1/2+d_{ox}/d)$, where ε_0, ε_r, d, t are

respectively the vacuum permittivity, dielectric constant, nanowire diamter and the thickness of gate oxide.[8] Under the metallic approximation, such method can be only applied to those heavily doped Si nanowires. Especially, due to the dielectric discontinuity in the back-gate configuration, an effective dielectric constant ε_{eff}=2.2 has to be used for the dielectric oxide of SiO_2 (ε_{SiO2}=3.9).[8] This treatment has been proved to provide good approximations to the real device capacitance as that from finite element method (FEM) simulations. [10] A representative comparison between the analytical method and the FEM simulation was shown in figure S4-c, and the careful examination of the dielectric constant is very important in the analytical method, as shown in Figure S5 (c).

Figure S5 (d) shows the hole mobility data as a function of the nanowire diameter. In contrast to the case of InAs nanowires,[11] there was no clear diameter dependence for the present Si nanowires. In figure S5 (e), the extracted mobility was further plotted as a function of the carrier concentration, which was calculated by the measured resistivity and mobility, as $p=1/\rho\mu e$. The result shows the clear trend, which is consistent with the impurity scattering limited carrier mobility in the heavily doped range (where the carriers are degenerated), and the hole mobility solely decreases with increasing the doping concentration.

7. Carrier redistribution under dopant inhomogeneity

In the presence of dopant inhomogeneity (heavily doped outer shell and lightly doped inner core), the activated carriers (holes in this case) would exhibit the non-uniform spatial distribution within the nanowire. As seen in *pn* junction, the carrier diffusion should occur across the inhomogeneous region until the Fermi level is aligned. By considering the diffusion and drift current, we performed simple calculations to simulate the carrier redistribution within our nanowires. The results of the dopant and hole distribution, the electrical field and potential profiles were shown in Figure S6. Since we do not have the dopant profile data in our Si nanowires, the present simulations can give only qualitative information. The finite element analysis was performed for above simulations. Si nanowire with the diameter of 100nm was simulated. First, a diffusion model was used to approach the dopant profile of B atoms in Si nanowires. The initial dopant concentration at the core was assumed to be $10^{16}cm^{-3}$, while the surface dopant concentration was set to be constant as $10^{20}cm^{-3}$. A diffusion constant of D=5x$10^{-16}cm^2/s$ for B atom in Si and a diffusion time of 600s was used in the simulation to approximate the experiment conditions.[12] The obtained dopant profile exhibited the characteristic of a heavily doped outer shell and the lightly doped inner core, as shown in Figure S6 (a). To simulate the hole redistribution, the electrostatic model was used. The surface potential of nanowire was assumed to be 0. The results indicated that the active hole concentration in the core region of nanowire was increased by an order compared to the initial doping level.

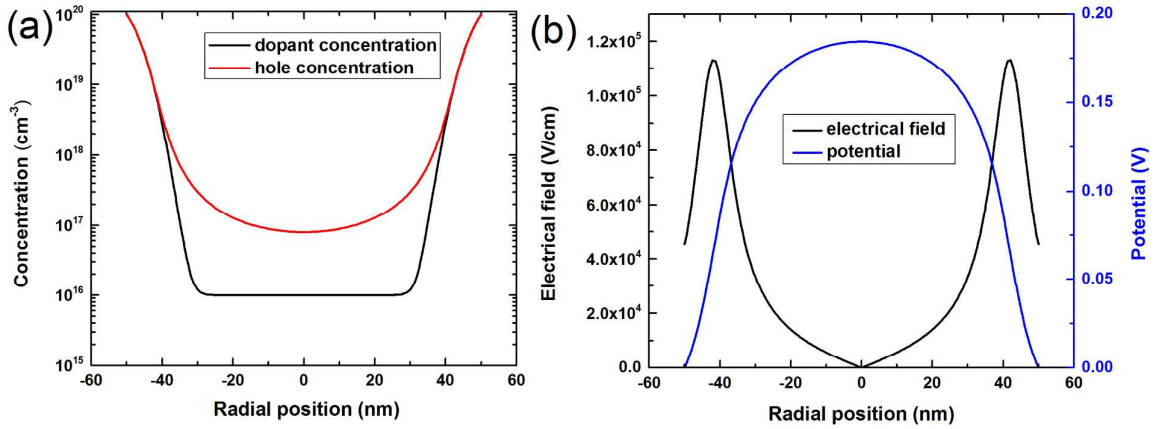

Figure S6. (a) Simulated radial profile of the dopant atoms and active holes. (b) The corresponding electrical field and potential profile in the same simulation.

In above simulations, the initial dopant profile would significantly influence the carrier redistribution in the equilibrium states. Here, we assumed the difference in the four orders of magnitude for the concentration of the surface and core dopant atoms, which came from the different incorporation efficiency from the nanowire surface and catalyst.[13] Since the wide distribution of over 5 orders on the nanowire resistivity was observed in our experiments, the above initial assumption on the dopant profile was expected to be reasonable.

8. Additional results for surface etching experiments

In Table 1 of the main manuscript, we showed the data of enhanced hole mobility after slightly removing the surface layer. The corresponding SEM morphology and the details of field effect measurements were shown in Figure S7. The increased slope of dI_{ds}/dV_g in Figure S7 (d), when compared with Figure S7 (c), directly indicates the higher hole mobility of the inner core than the outer layer. Considering that the hole mobility in present Si nanowires were generally limited by the impurity scattering, this result can therefore be the evidence as to the presence of heavily doped outer shell and the lightly doped inner core for the present VLS grown B-doped Si nanowire.

Figure S8 shows the resistance variation results of Si nanowires when we performed various surface etching steps. All resistance data of Si nanowires were normalized to the nanowire length, $R_{normalized}=R/L=4\rho/\pi d^2$. The dash lines in the figure were used to indicate the expected results from uniform dopant profiles- *i.e.* constant resistivity. A fixed surface density of states D_{it}=1x10^{12}cm^{-2} was assumed on the Si nanowire after the SC1 surface etching.[14] The surface depletion effect was

considered by following the earlier reference.[15] As seen in the figure, the samples with the smaller diameter or the lighter doping concentration showed the more significant surface effects on the measured electrical properties. However, even considering the surface depletion, our experiment results of surface etching showed the apparent deviation from the expectation of uniform dopant profile. From many similar etching experiments, we conclude that the thin surface layer in present VLS grown B-doped Si nanowires plays a major role on the transport carriers for total electrical conduction.

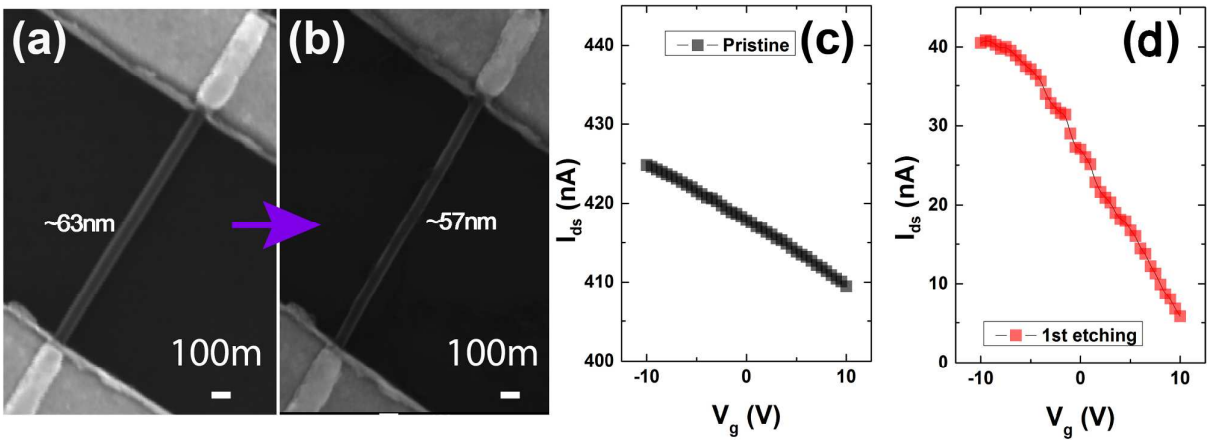

Figure S7. Additional details for the surface etching experiment shown in table 1 of the main manuscript: (a), (b) the morphology and (c), (d) the transconductance measurement.

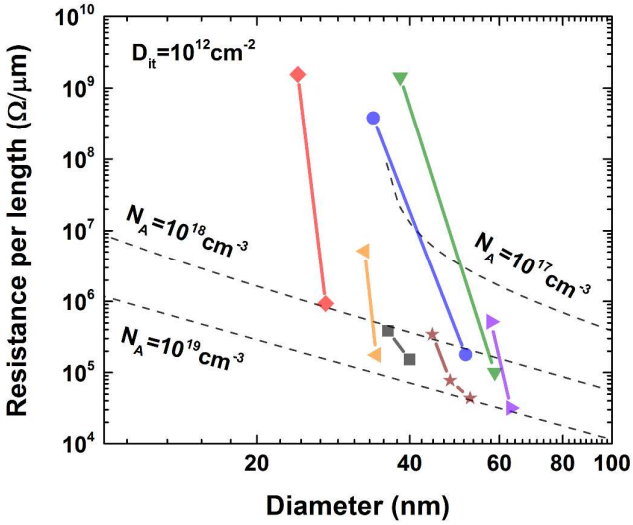

Figure S8. The resistance (normalized) variation after surface etching (each marker here corresponds to the same nanowire device). The dash lines are used to indicate the expectations from uniform dopant profile, by considering different doping concentration but a fixed surface states of D_{it}~1x$10^{12}$$cm^{-2}$.

9. TEM images of δ-doped Si nanowire

Figure S9 shows the TEM images of δ-doped Si nanowires, which were fabricated by growing a heavily B-doped Si layer on non-doped VLS grown Si nanowires. The lattice fringe and diffraction pattern in figure S9 b and c suggested that the nanowires were <111> oriented. From the images of several nanowires, the surface shell layer on δ-doped Si nanowires was estimated to be around 2~5nm.

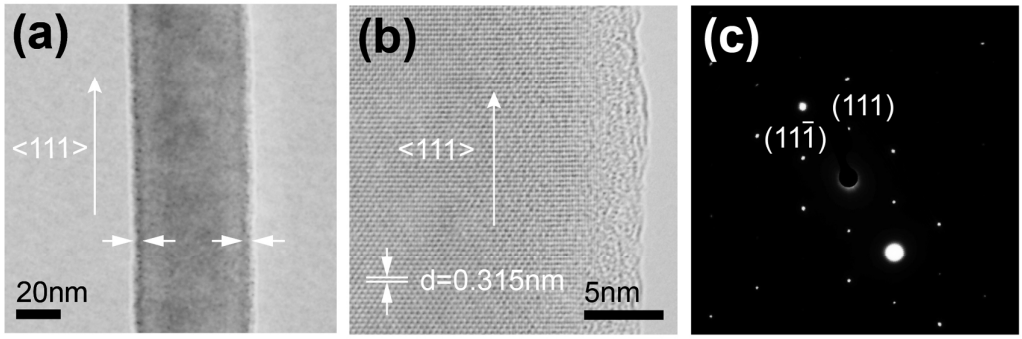

Figure S9. (a), (b) and (c), the low, high magnification TEM image and selective area electron diffraction (SAED) pattern of a δ-doped Si nanowire.

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