Supporting Information

Spatial Nonuniformity in Resistive-Switching Memory Effects of NiO

Keisuke Oka[1], Takeshi Yanagida[1,2]*, Kazuki Nagashima[1], Masaki Kanai[1] and Tomoji Kawai[1,3]*,

Jin-Soo Kim[3] and Bae Ho Park[3]

1 Institute of Scientific and Industrial Research, Osaka University, 8-1 Mihogaoka Ibaraki, Osaka, 567-0047, Japan

2 PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho Kawaguchi, Saitama, 332-0012, Japan

3 Division of Quantum Phases & Devices, Department of Physics, Konkuk University, Seoul 143-701, Korea

* E-mail: yanagi32@sanken.osaka -u.ac.jp, kawai@sanken.osaka-u.ac.jp.

1. Fabrication process of Pt/NiO nanowire/Pt Junctions

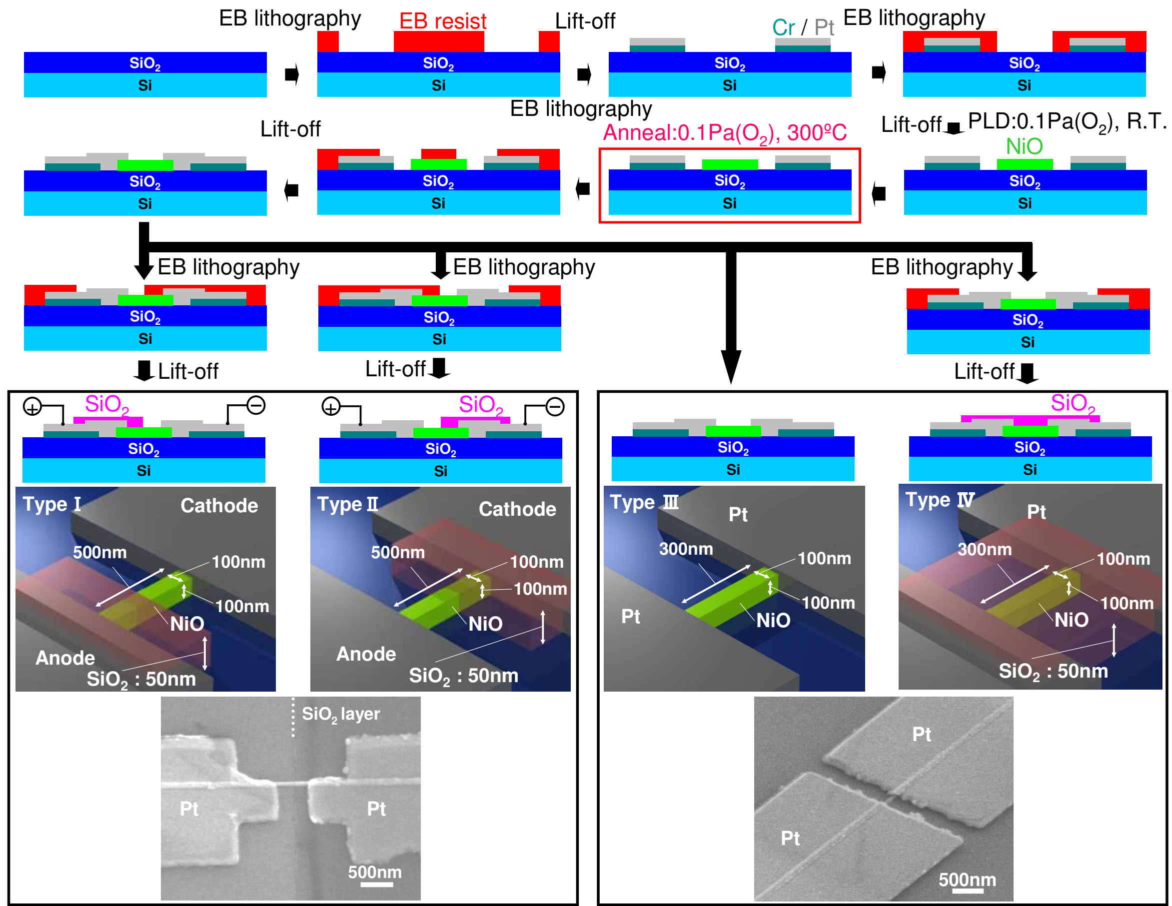

Figure S1. Schematic diagram of device fabrication process.

Figure S1 shows the schematic diagram of device fabrication process and the FESEM images of fabricated planer Pt/NiO nanowire/Pt junctions. First, the electrodes were formed by an electron beam (EB) lithography. The resist for EB lithography was composed of ZEP-520A7 (ZEONREX Electronic Chemicals). After EB lithography patterning, Pt/Cr (70 nm/5 nm) as two phase electrodes were deposited by RF sputtering. Pt was utilized because of the relatively high melting point (1769 ^{o}C) not only for the annealing in the fabrication process but also for the operations at high temperature elevated by the current injections into nano-channels, when compared with typical Au (the melting point 1063°C). Cr was used as the adhesive layer between Pt and SiO_2/Si substrate. The gap spacing of fabricated electrodes was typically 500nm for Type I and Type II junctions and 300 nm for Type III and Type IV junctions. Second, NiO nanowire was formed onto the EB patterned substrate by using pulsed laser

deposition (PLD) technique. NiO pellet (99.9% pure) was used as the target. The background pressure of the chamber was less than 5×10^{-6} Pa. The deposition was performed under room temperature and 10^{-1} Pa of the oxygen pressure (oxygen gas: 99.9999% pure). The laser energy, the repetition rate, and the distance between the substrate and the target source were set to 40 mJ, 10 Hz, and 45 mm, respectively. The thickness was controlled to be around 100 nm (growth rate: ~0.56 nm/min). After the construction of NiO nanowire, the amorphous SiO2 passivation layer with 50 nm thickness was deposited onto the desired spatial location by the combined process of RF sputtering and EB lithography.

2. Microstructures of fabricated NiO nanowire junctions

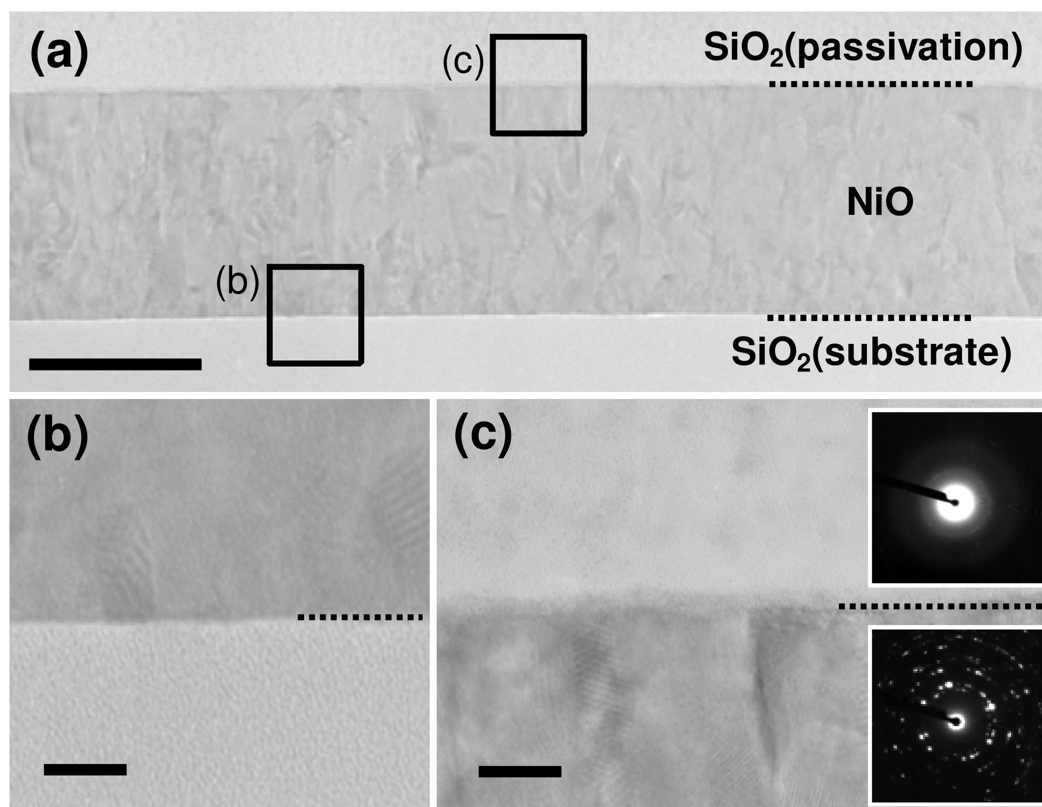

Figure S2. (a) Low magnification cross-sectional HRTEM image of fabricated NiO nanowire junction. The scale bar is 100 nm. (b) High magnification cross-sectional HRTEM image at the interface between NiO and the substrate (c) High magnification cross-sectional HRTEM image at the interface between NiO and amorphous SiO_2 passivation layer. The scale bar is 10 nm. Insets show the selected area electron diffraction (SAED) pattern of SiO_2 passivation and NiO.

High resolution transmission electron microscopy (HRTEM, JEM-3000F) at an accelerating voltage of 300 kV was used to evaluate the microstructures of SiO_2 passivation layer/NiO layer/ SiO_2/Si substrate. This structure corresponds to the planer type nanowire junctions fabricated for RS measurements. Figure S2 shows the cross-sectional TEM images of (a) low magnification and (b) (c) interfaces of the junctions. Selected area electron diffraction (SAED) pattern was used to characterize the crystal structures on passivation SiO_2 and NiO layers. SAED patterns have demonstrated that the fabricated SiO_2 is amorphous and NiO later is polycrystalline form.

3. Data of retention measurements and forming process

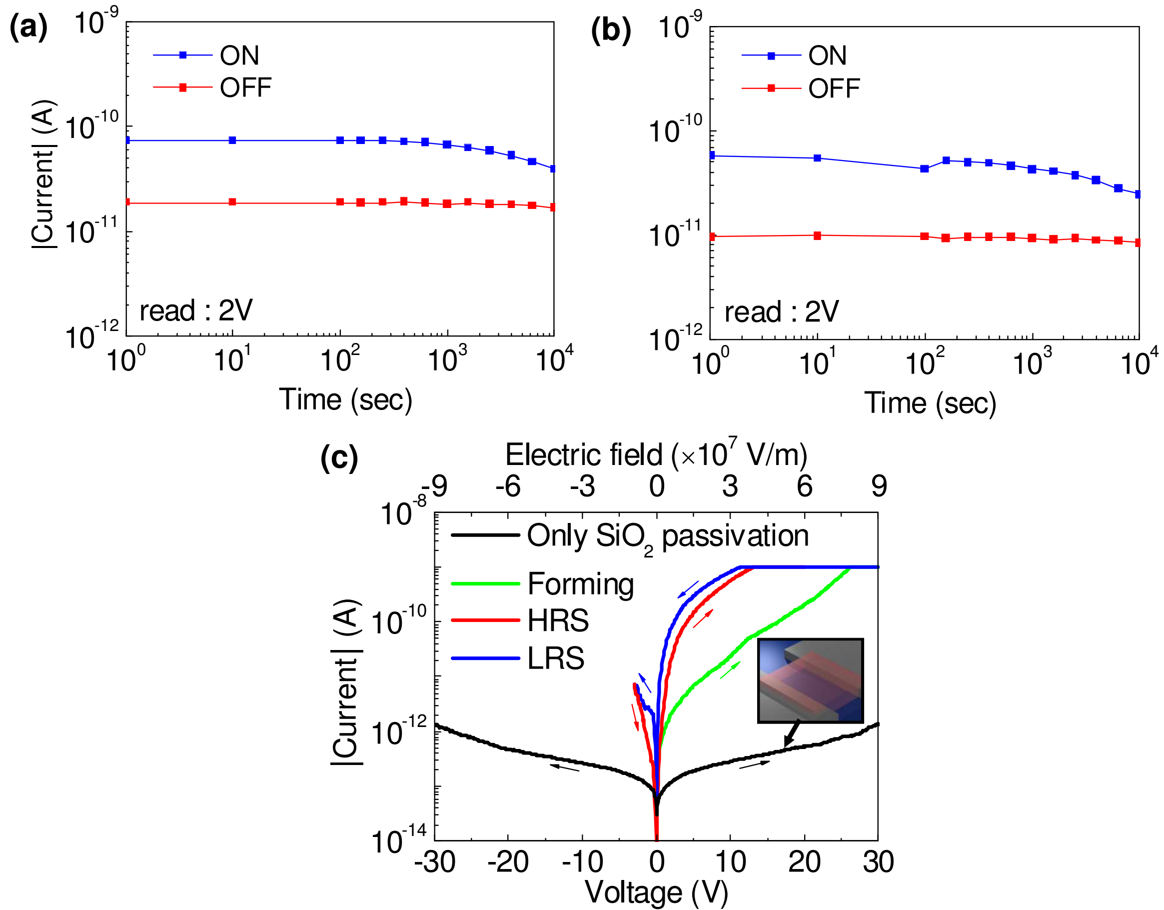

Figure S3. (a) Retention data of HRS and LRS for Type III junction. (b) Retention data of HRS and LRS for Type IV junction. (c) IV curves of Type IV junction, including the forming process and the background current data when only SiO_2 passivation layer existed without NiO nanowire in the junction.

Figure S3 (a) and (b) show the retention time data for two type junctions. The non-volatile properties between high resistance state (HRS) and low resistance state (LRS) can be seen at least up to 10^4 sec. The current was measured by applying the constant voltage of 2V. The ON/OFF ratio strongly depends on the value of compliance current used, because the ON resistance is defined by the compliance current. Since this study has concerned with identifying the bipolar RS mechanisms rather than showing the RS characteristics superior to previous data, we used the relatively low compliance current with the low ON/OFF ratio. In addition, the relative short retention time can be interpreted in terms of both the

low conductance of ON state in the present experiments and the nature of planar junctions exposed to atmosphere. Figure S3(c) shows *I-V* curves of forming, SET and RESET process from the pristine state. After so-called forming process, which is defined as the initial process to introduce the electrical conduction within pristine insulative matrix by high electric field, the devices exhibited the *I-V* curves in Figure 2. Note that the pristine resistance before forming process was almost the same value in all junctions. In addition, the black line shows the data in the case of only SiO_2 passivation layer in the junction as the background current. Since the background current is far less than the current of NiO nanowire junction, the current through the passivation layer must be negligible.

4. Comparison of p-type and n-type materials

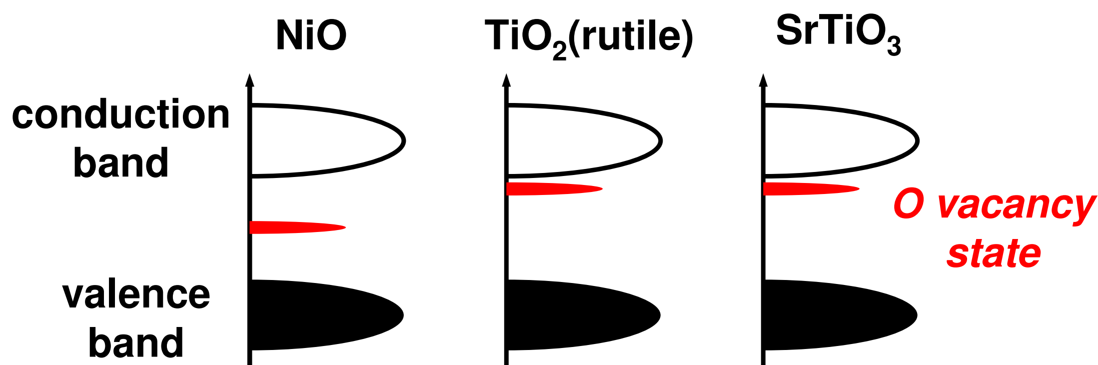

Figure S4. Schematic as to the material dependence in the energy levels of oxygen vacancies.

Figure S4 shows schematic of the material dependences in the energy levels of oxygen vacancies. In the case of NiO, which is typically p-type, the oxygen vacancy state is formed in the mid-gap state [14]. Thus in general oxygen vacancies cannot provide the electric conduction of NiO. On the other hand, in the cases of TiO_2 [17] and $SrTiO_3$ [12], which are typically n-type, the oxygen vacancy state is formed near the conduction band minimum, giving mobile electron carriers via thermal excitation.

5. Reproducibility of each devices

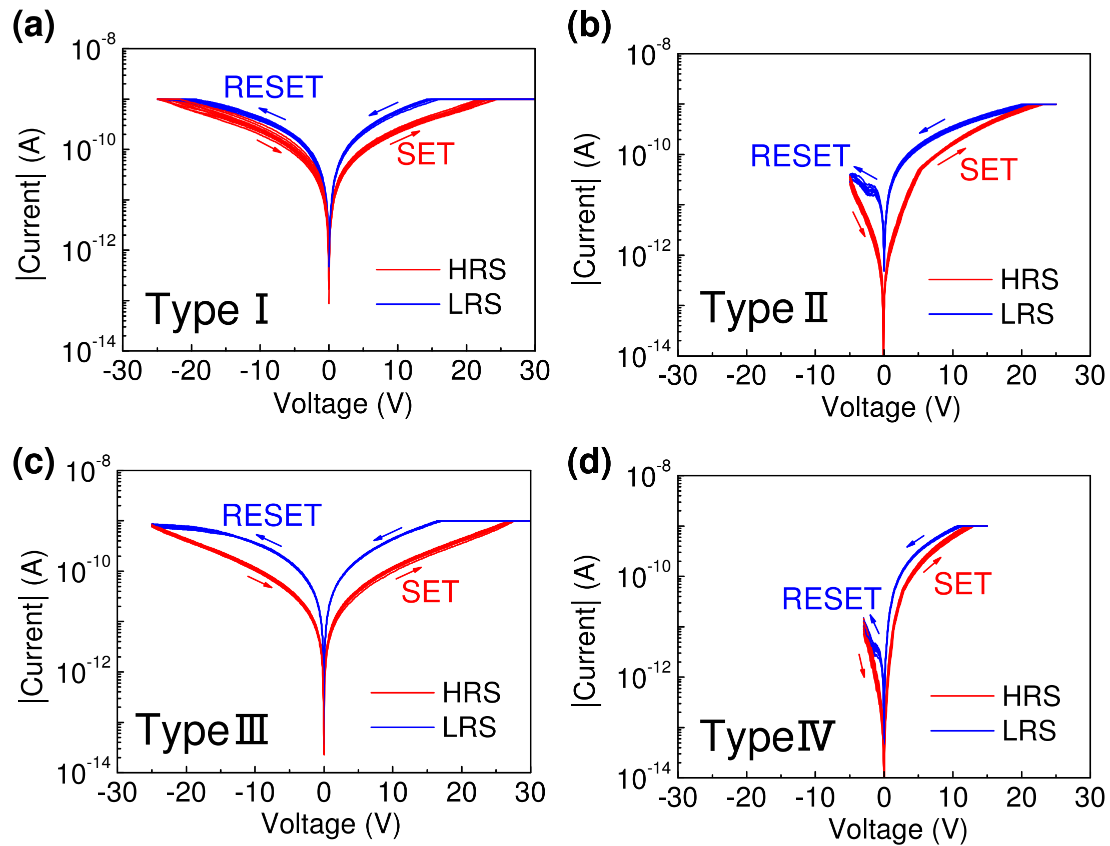

Figure S5. *I-V* curves of 10 cycles of (a) Type I junction, (b) Type II junction, (c) Type III junction and (d) Type IV junction. In the figures, high resistance state (HRS) and low resistance state (LRS) are highlighted by red and blue, respectively.

6. Evaluation of SiO_2 layer effects in the vacuum state

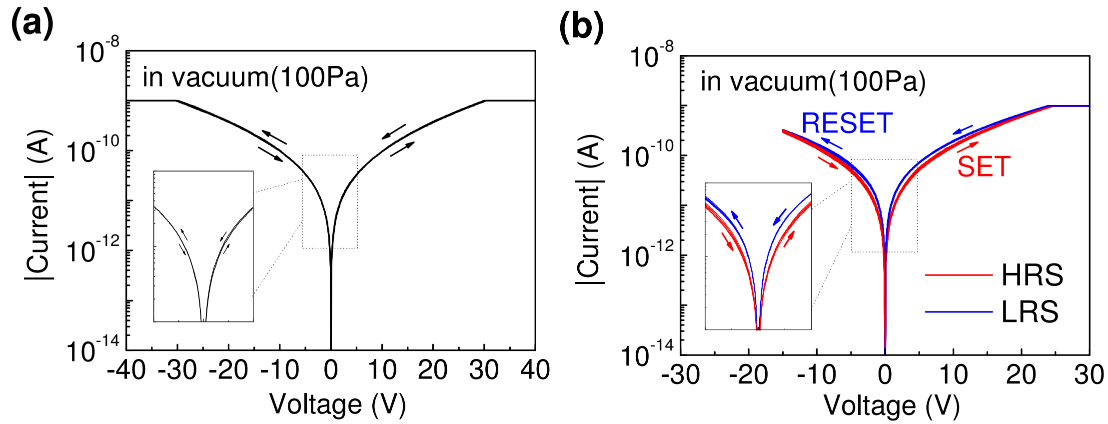

Figure S6. Typically *I-V* curves of (a) Type III junction and (b) Type IV junction in 100Pa vacuum state. Inset shows enlarged I-V curves. In the figures, high resistance state (HRS) and low resistance state (LRS) are highlighted by red and blue, respectively.

We have performed experiments in the vacuum state (we have performed the pumping to reduce the pressure from atmospheric pressure to 100Pa) to investigate the effect of SiO_2 passivation layer as the source of surrounding oxygen. In the vacuum state, the memory effects were not observed in the case of Type III junction without passivation layer. On the other hand, Type IV junction with SiO_2 passivation layer showed the bipolar switching memory effects even in the vacuum state. Thus this result indicates that SiO_2 passivation layer can play a role of the source of surrounding oxygen as expected.

7. Comparison of electric field intensity between planer and capacitor type devices

Device structure	Planar type	Planar type	Capacitor type
Effective cell size (nm^2)	100×100	50×50	100×100
Electric field intensity required for resistive switching (V/cm)	5.40×10^5	4.29×10^5	6.00×10^5

Table S1. Comparison of electric field intensity required for resistive switching when varying device geometry, device structure and effective cell size.

Table S1 shows the electric field intensity required for resistive switching when varying device structures, the cell size in the bipolar operation of NiO. The present planar devices are comprised of the gap between electrodes (300-500nm), which is in fact ten times longer than the typical gap of capacitor devices. This large electrode gap requires high voltages to be SET or RESET to achieve the electric field intensity required for the switching. We also confirmed the consistency between the present planar junctions and the capacitor junctions of NiO in terms of the electric field intensity, as shown in Table S1.

Complete Ref. 2a and 2b in manuscript

(a) Lee, M.; Kim, S. I.; Lee, C. B.; Yin, H.; Ahn, S.; Kang, B. S.; Kim, K. H.; Park, J. C.; Kim, C. J.; Song, I.; Kim, S. W.; Stefanovich, G.; Lee, J. H.; Chung, S. J.; Kim, Y. H.; Park, Y. *Adv. Funct. Mater.* **2008**, *18*, 1.

(b) Ahn, S.; Lee, M.; Park, Y.; Kang, B. S.; Lee, C. B.; Kim, K. H.; Seo, S.; Suh, D.; Kim, D.; Hur, D.; Xianyu, W.; Stefanovich, G.; Yin, H.; Yoo, I.; Lee, J.; Park, J.; Baek, I.; Park, B. H. *Adv. Mater.* **2008**, *20,* 924.