Non-volatile Bipolar Resistive Memory Switching in Single Crystalline NiO Heterostructured Nanowires

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Supporting Information

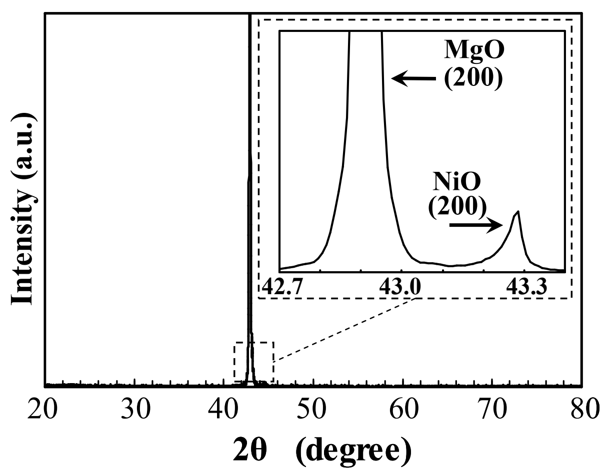

Figure S1. XRD data of the NiO/MgO heterostructured nanowires grown on MgO (100) single crystal substrate. The NiO shell layer was formed at 10 Pa of the oxygen pressure and 800^{o}C of the growth temperature.

Figure S1 shows the XRD data of the NiO/MgO heterostructured nanowires grown on MgO (100) single crystal substrate. The formation conditions for the NiO shell layers were 10 Pa of the oxygen pressure and 800^{o}C of the growth temperature, respectively. The presence of the NiO (200) peak clearly indicates the preferential orientation of the NiO heterostructured nanowires along the direction perpendicular to the MgO single crystal substrate. Thus the NiO shell layers were epitaxially grown on the MgO core nanowires. The single crystalline nature of NiO heterostructured nanowires was further confirmed by performing the high-resolution TEM analysis as shown in Figure S2. The HRTEM image clearly indicates the single crystalline nature of fabricated NiO heterostructured nanowires.

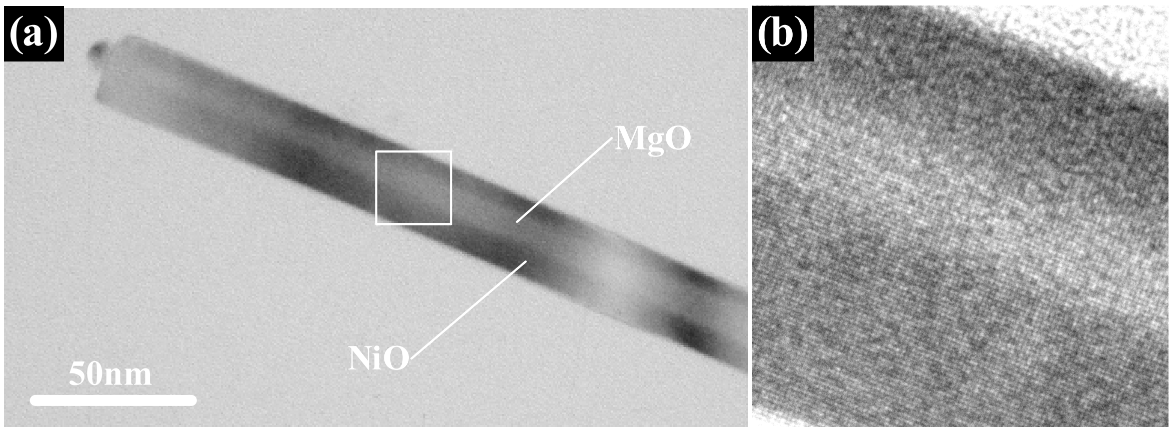

Figure S2. HRTEM images of NiO/MgO heterostructured nanowire.

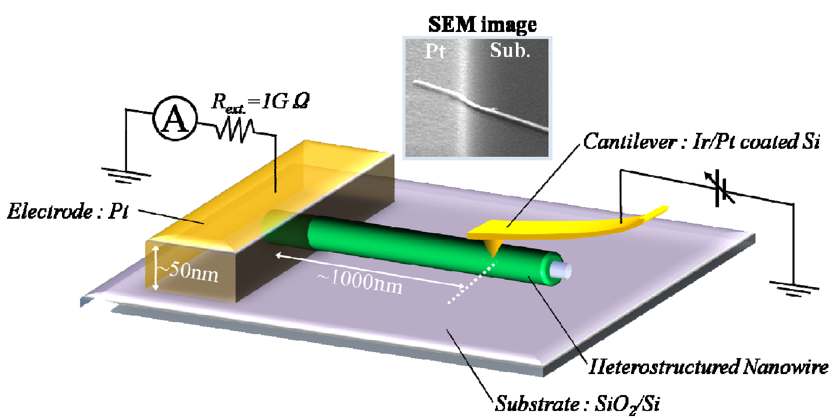

Figure S3. Schematic diagram of C-AFM measurement system.

Figure S3 shows the schematic diagram of C-AFM measurements employed. The used cantilever was conductive Ir/Pt coated Si (Nanoworld). The C-AFM measurements were performed at the nanowire position around 1000nm away from Pt electrode. The Pt electrode was fabricated by using the mask of cleavage Si substrate. The external resistance (1GΩ) was used to prevent the permanent breakdown of the NiO heterostructured nanowires when SET occurs. The C-AFM measurements were always performed after confirming the exact location of the NiO heterostructured nanowires using non-destructive tapping-mode. The typical cross-sectional area of NiO in the heterostructured nanowires was 10^{-3}μm^2. The formation conditions for NiO shell layers were 300C of the growth temperature and 0.1Pa of the oxygen pressure, considering the NiO conductivity in previous investigations using NiO hetero-thin films [20]. We have performed several experiments to confirm the occurrence of the resistive switching within the NiO layer. First, the I-V measurement between the substrate and the electrode was performed, which exhibited only noise-level current below 10^{-12}A. Second, the I-V measurement using more conductive NiO layer grown under reduced atmosphere (300C of the temperature and 10^{-3}Pa of the oxygen pressure: see also the reference [18]) was performed. We confirmed the bipolar resistive switching with the lower ON/OFF ratio and the increase of the measured current on the OFF state. This result clearly indicates the contribution of NiO layer conductivity on the measured I-V data. Third, the I-V measurement on bare MgO nanowire was performed. Only noise-level current below 10^{-12}A was obtained due to the insulating nature of MgO. In addition, the initial resistance of the device- $10^{11}\Omega$ was almost consistent with the resistance estimated theoretically from the NiO thin film resistivity. [18] Furthermore the switching electric field of the nanowire device was almost consistent with the switching electric field of the NiO epitaxial thin film devices with the bipolar switching. Thus these experimental results consistently indicate the occurrence of the resistive switching within the NiO layer. Figure S4 shows the I-V curves for two cycles, the retention and the endurance data of the device. The retention time was at least over 10^4s, and the endurance was confirmed for 6 cycles until the Pt coating on the AFM tip was deteriorated due to applying the high voltage sweep. These data clearly indicate the non-volatile memory effect of the device. The switching is not a threshold switching, in which there is no non-volatile memory effect. In such case, the resistance of the device is always high once after the applied voltage was stopped. On the other hand, in our case after the SET process, the low resistance of the device was kept as long as the voltage sweep was performed on the same polarity. This memory effect was kept even if the voltage sweep was applied once after the applied voltage was stopped. Once applying the inverse polarity voltage sweep, the RESET process appeared. Thus observed phenomenon is a bistable memory switching.

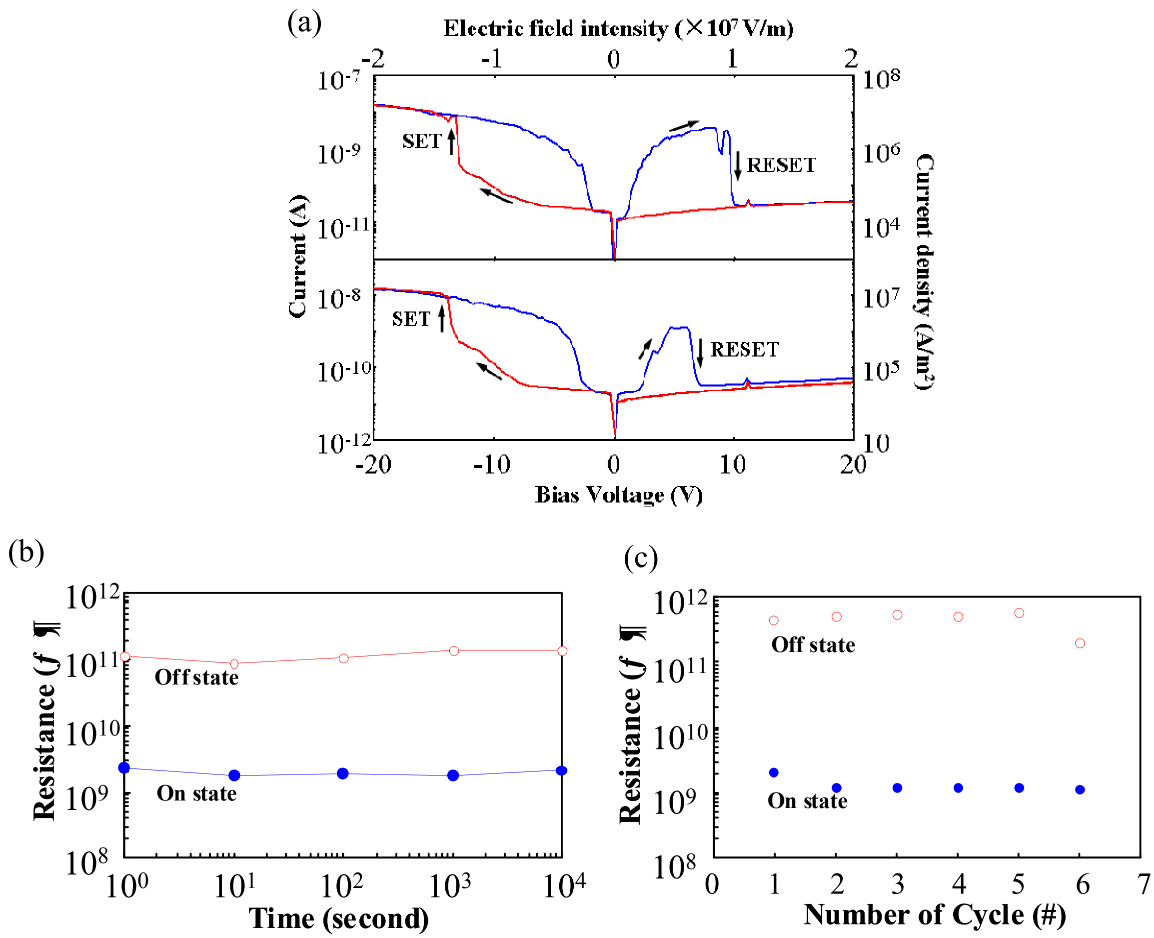

Figure S4. I-V curves, retention and endurance data of the device.

Supporting information in References

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(14) Ahn, S.-E.; Lee, M.-J.; Park, Y.; Kang, B. S.; Lee, C. B.; Kim, K. H.; Seo, S.; Suh, S.-S.; Kim D.-C.; Hur, J.; Xianyu, W.; Stefanovich, G.; Yin, H.; Yoo, I.-K.; Lee, J.-H.; Park, J.-B.; Baek, I.-G.; Park, B. H. *Adv. Mater.* **2008**, 20, 924-928.